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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/673,501 | 09/30/2003 | Andrej S. Mitrovic | 230421US6YA | 2312 |

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| SAXENA, AKASH | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2128 | |

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/673,501 | MITROVIC, ANDREJ S. | |
| | Examiner | Art Unit | |
| | Akash Saxena | 2128 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-62 have been presented for examination based on the application filed on 30th September 2003.

### *Specification*

2. Claims 46-47 are objected because of improper dependency.

MPEP § 608.01(n) states:

> A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.
> A claim, which depends from a dependent claim, should not be separated by any claim, which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 48 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 48 discloses "computer readable medium" which is defined in the specification (Pg.32-33 [00103] Line1-9) to include tangible items ("non volatile media" and "volatile media") and items that are non-tangible ("transmission media"). Therefore the claim as whole is not directed towards a tangible medium. One possible suggested way to overcome this rejection is to replace "computer readable medium" with "non volatile media" and "volatile media".

***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

**4. Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,583.**

| Application No. 10/673,501 | Application No. 10/673,583 |
|---|---|
| A method of facilitating a process performed by a semiconductor processing tool, comprising: | A method of facilitating a process performed by a semiconductor processing tool, comprising: |
| inputting data relating to a process performed by the semiconductor processing tool; | inputting data relating to a process performed by the semiconductor processing tool; |
| inputting a first principles physical model relating to the semiconductor processing tool; | inputting a first principles physical model relating to the semiconductor processing tool; |
| performing first principles simulation using the input data and the physical model to provide a simulation result for the process performed by the semiconductor processing tool; and | performing first principles simulation using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and |
| using the simulation result as part of a data set that characterizes the process performed by the semiconductor processing tool. | using the virtual sensor measurement to facilitate the process performed by the semiconductor processing tool. |

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). Further, the process of facilitating could be a

characterization the semiconductor fabrication process (Specification: Page 6[0032] Lines 1-5). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,138.**

| Application No. 10/673,583 | Application No. 10/673,138 |
|---|---|
| A method of facilitating a process performed by a semiconductor processing tool, comprising: | A method of facilitating a process performed by a semiconductor-processing tool, comprising: |
| inputting data relating to a process performed by the semiconductor processing tool; | inputting data relating to a process performed by the semiconductor processing tool; |
| inputting a first principles physical model relating to the semiconductor processing tool; | inputting a first principles physical model relating to the semiconductor processing tool; |
| performing first principles simulation using the input data and the physical model to provide a simulation result for the process performed by the semiconductor processing tool; and | performing first principles simulation using the input data and the physical model to provide a first principles simulation result; and |
| using the simulation result as part of a data set that characterizes the process performed by the semiconductor processing tool. | using the first principles simulation result to facilitate the process performed by the semiconductor processing tool. |

Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims perform the same steps and use the simulation result to facilitate the semiconductor-processing tool. Characterization is also same as facilitating (Specification: Page 6[0032]). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Further, all the two non-statutory obviousness-type double patenting rejections for the application have substantially same or identical specification. Also, independent claims belonging different statutory category, having substantially similar limitations, in the three co-pending applications may also have similar double patenting rejections.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**6. Claims 1-48 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter).**

Regarding Claim 1

Sonderman teaches a method to facilitate a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting data relating to the process performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation using the input data and the physical model to provide simulation results for the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the simulation results as part of the data set that characterize the process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8).

Regarding Claim 2

Sonderman teaches directly inputting the data relating to the process performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the data relating to the process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7).

Regarding Claim 6

Sonderman teaches inputting data related to process performed by semiconductor processing tool as virtual sensor data (Sonderman: at least in Col.5-7; parameters).

Regarding Claims 7-10

Sonderman teaches inputting data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment; inputting data relating to at least on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result that can form part of the data set

that characterizes the process performed by the semiconductor processing tool (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3).

Regarding Claim 11

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claim 12

Sonderman teaches performing first principle simulation to provide a simulation result that is a variation of parameter tested by the concurrent process performed by the semiconductor-processing tool (Sonderman: at least in Col.7 Lines 21-Col.8 Line 27).

Regarding Claim 13

Sonderman teaches performing first principle simulation to provide a simulation result relating to a different parameter than a parameter tested by the concurrent process performed by the semiconductor-processing tool (Sonderman: Col.5 Line 56 – Col.6 Line 34; changes to various parameters/characteristics of different model/inter-model dependency).

Regarding Claims 14

Sonderman teaches performing first principle simulation not concurrently with the process performed; inputting data from at least one initial condition recorded from a previous process performed (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 15

Sonderman teaches storing data set in a library (as updated model) for subsequent use processes performed by the semiconductor-processing tool (Sonderman: Fig.5 Col.7 Lines 21-55).

Regarding Claims 16-20

Sonderman teaches using a network of interconnected resources to perform at least one of the process steps recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 21-22

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 23

System claim 23 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 24

System claim 24 discloses substantially similar limitations as method claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 25-27

System claims 25-27 disclose substantially similar limitations as method claims 3-5 and are rejected for the same reasons as claims 3-5.

Regarding Claim 28

System claim 28 discloses substantially similar limitations as method claim 6 and is rejected for the same reasons as claim 6.

Regarding Claims 29-32

System claims 29-32 disclose substantially similar limitations as method claims 7-10 and are rejected for the same reasons as claims 7-10.

Regarding Claim 33

System claim 33 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claim 34

System claim 34 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 35

System claim 35 discloses substantially similar limitations as method claim 13 and is rejected for the same reasons as claim 13.

Regarding Claim 36

System claim 36 discloses substantially similar limitations as method claim 14 and is rejected for the same reasons as claim 14.

Regarding Claim 37

System claim 37 discloses substantially similar limitations as method claim 15 and is rejected for the same reasons as claim 15.

Regarding Claims 38-42

System claims 38-42 disclose substantially similar limitations as method claims 16-20 and are rejected for the same reasons as claims 16-20.

Regarding Claims 43-44

System claims 43-44 disclose substantially similar limitations as method claims 21-22 and are rejected for the same reasons as claims 21-22.

Regarding Claim 45

System claim 45 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 46

System claim 46 discloses substantially similar limitations as method claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 47

System claim 47 discloses substantially similar limitations as method claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 48

System claim 48 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

## *Conclusion*

7. All claims are rejected.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

***Communication***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner GAU 2128
(571) 272-8351
Thursday, August 18, 2005

Fred Ferris
GAU 2128